CLAIMS

26. Memory circuitry comprising:

a semiconductor substrate;

a plurality of word lines received over the semiconductor substrate;

an insulative layer received over the word lines and the substrate, the insulative layer having at least one well formed therein, the well comprising a base received over the word lines, the well peripherally defining an outline of a memory array area, area peripheral to the well comprising memory peripheral circuitry area;

a plurality of memory cell storage capacitors received within the well over the word lines; and

peripheral circuitry within the peripheral circuitry area operatively configured to write to and read from the memory array.

27. The memory circuitry of claim 26 wherein the base is substantially planar.

28. The memory circuitry of claim 26 wherein the word lines have insulative caps and the well base has a lowest portion which is received at least 2000 Angstroms above the caps.

29. The memory circuitry of claim 26 comprising buried digit lines, the well base having a lowest portion which is received at least 1000 Angstroms above outermost tops of the digit lines.

30. The memory circuitry of claim 26 comprising buried digit lines and wherein the base is substantially planar, and the well base being received at least 1000 Angstroms above outermost tops of the digit lines.

31. The memory circuitry of claim 26 wherein the insulative layer has a substantially planar outermost surface, and the capacitors have capacitor storage node electrodes having topmost surfaces received elevationally proximate the substantially planar outermost surface of the insulative layer.

32. The memory circuitry of claim 26 wherein the insulative layer is formed to have a substantially planar outermost surface, and the capacitors have capacitor storage node electrodes having topmost surfaces received elevationally above the substantially planar outermost surface of the insulative layer by less than 50 Angstroms.

33. Memory circuitry comprising:

a semiconductor substrate;

an insulative layer received over the substrate, the insulative layer having at least one well formed therein, the well peripherally defining an outline of a memory array area, area peripheral to the well comprising memory peripheral circuitry area, the well having a substantially planar base;

a plurality of memory cell storage capacitors received within the well, the memory cell storage capacitors respectively comprising a storage node container which is received partially within the insulative layer through the well base; and

peripheral circuitry within the peripheral circuitry area operatively configured to write to and read from the memory array.

34. (Amended) The memory circuitry of claim 33 comprising word lines, wherein the word lines have insulative caps and the well base has a lowest portion which is received at least 2000 Angstroms above the caps.

35. The memory circuitry of claim 33 comprising buried digit lines, the well base having a lowest portion which is received at least 1000 Angstroms above outermost tops of the digit lines.

36. The memory circuitry of claim 33 wherein the insulative layer has a substantially planar outermost surface, and the capacitors have capacitor storage node electrodes having topmost surfaces received elevationally proximate the substantially planar outermost surface of the insulative layer.

37. The memory circuitry of claim 33 wherein the insulative layer is formed to have a substantially planar outermost surface, and the capacitors have capacitor storage node electrodes having topmost surfaces received elevationally above the substantially planar outermost surface of the insulative layer by less than 50 Angstroms.

38. Dynamic random access memory circuitry comprising:

a semiconductor substrate;

word lines received over the semiconductor substrate;

an insulative layer received over the word lines and the substrate, the insulative layer having at least one well formed therein, the well comprising a base received over the word lines, the well peripherally defining an outline of a memory array area, area peripheral to the well comprising memory peripheral circuitry area, the well having a substantially planar base;

a plurality of memory cell storage capacitors received within the well, the memory cell storage capacitors respectively comprising a storage node container

which is received partially within the insulative layer through the well base over the word lines; and

peripheral circuitry within the peripheral circuitry area operatively configured to write to and read from the memory array.

39. The memory circuitry of claim 38 wherein the insulative layer has a substantially planar outermost surface, and the capacitors have capacitor storage node electrodes having topmost surfaces received elevationally proximate the substantially planar outermost surface of the insulative layer.

40. The memory circuitry of claim 38 wherein the insulative layer is formed to have a substantially planar outermost surface, and the capacitors have capacitor storage node electrodes having topmost surfaces received elevationally above the substantially planar outermost surface of the insulative layer by less than 50 Angstroms.

41. The memory circuitry of claim 38 comprising buried digit lines, the well base having a lowest portion which is received at least 1000 Angstroms above outermost tops of the digit lines.

42. Dynamic random access memory circuitry comprising:

a semiconductor substrate;

word lines received over the semiconductor substrate;

bit lines received over the word lines;

an insulative layer received over the word lines, the digit lines and the substrate, the insulative layer having at least one well formed therein, the well comprising a base received over the word lines and the digit lines, the well peripherally defining an outline of a memory array area, area peripheral to the well comprising memory peripheral circuitry area;

a plurality of memory cell storage capacitors received within the well over the word lines and the digit lines; and

peripheral circuitry within the peripheral circuitry area operatively configured to write to and read from the memory array.

43. The memory circuitry of claim 42 wherein the insulative layer has a substantially planar outermost surface, and the capacitors have capacitor storage node electrodes having topmost surfaces received elevationally proximate the substantially planar outermost surface of the insulative layer.

44. The memory circuitry of claim 42 wherein the insulative layer is formed to have a substantially planar outermost surface, and the capacitors have capacitor storage node electrodes having topmost surfaces received elevationally above the substantially planar outermost surface of the insulative layer by less than 50 Angstroms.

45. Dynamic random access memory circuitry comprising:

a semiconductor substrate;

word lines received over the semiconductor substrate;

bit lines received over the word lines;

an insulative layer received over the word lines, the digit lines and the substrate, the insulative layer having at least one well formed therein, the well comprising a substantially planar base received over the word lines and the digit lines, the well peripherally defining an outline of a memory array area, area peripheral to the well comprising memory peripheral circuitry area;

a plurality of memory cell storage capacitors received within the well, the memory cell storage capacitors respectively comprising a storage node container which is partially received within the insulative layer through the well base; and

peripheral circuitry within the peripheral circuitry area operatively configured to write to and read from the memory array.

46. The memory circuitry of claim 45 wherein the insulative layer has a substantially planar outermost surface, and the capacitors have capacitor storage node electrodes having topmost surfaces received elevationally proximate the substantially planar outermost surface of the insulative layer.

47. The memory circuitry of claim 45 wherein the insulative layer is formed to have a substantially planar outermost surface, and the capacitors have capacitor storage node electrodes having topmost surfaces received elevationally above the substantially planar outermost surface of the insulative layer by less than 50 Angstroms.